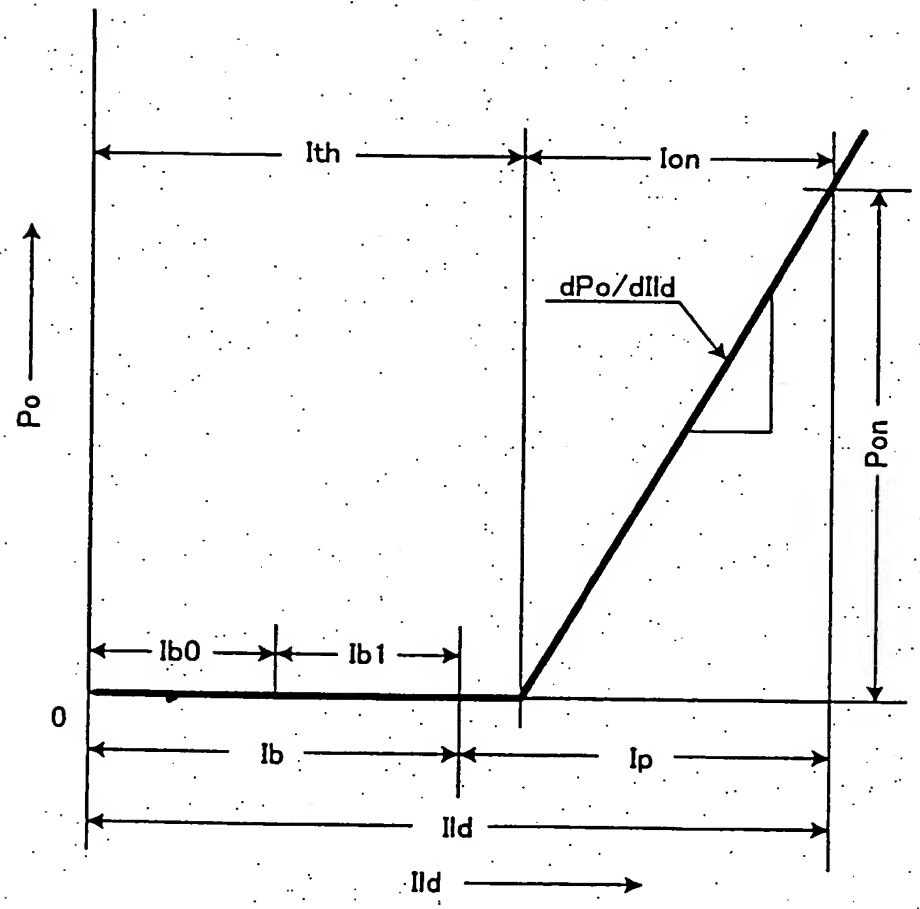


FIG. 1

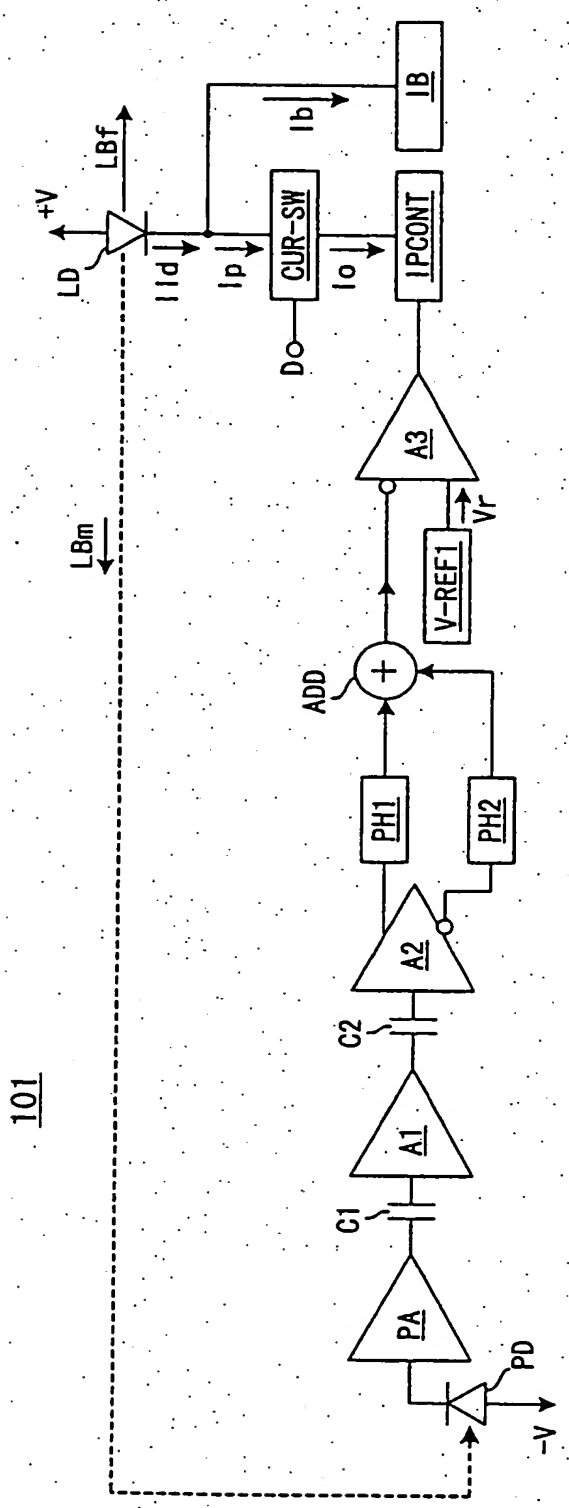

101
LBf
+V
LD
Ild
Ip
CUR-SW
Io
IPCONT
Ib
IB
Do
A3
Vr
V-REF1
LBm
ADD
PH1
PH2
A2
C2
A1
C1
PA
PD
-V

FIG. 2

FIG. 3

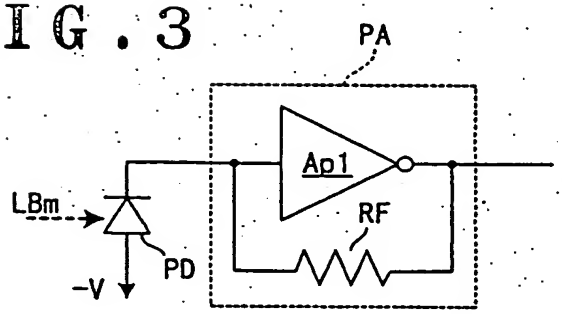


FIG. 4

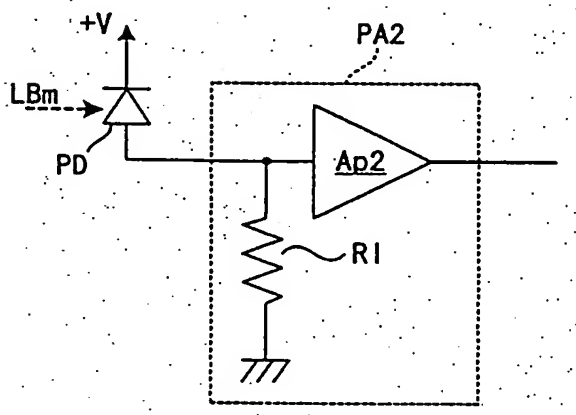


FIG. 5A

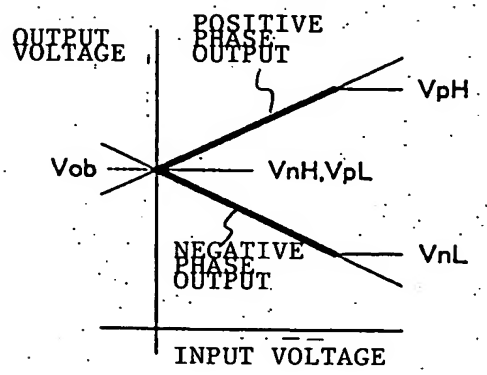


FIG. 5B

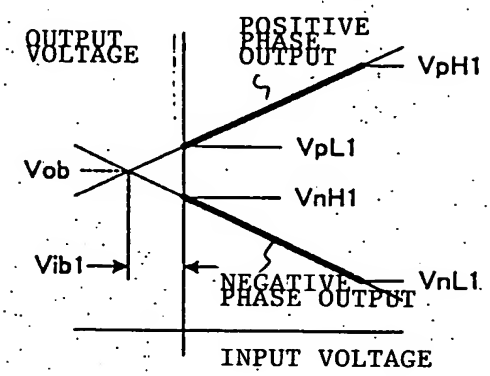


FIG. 5C

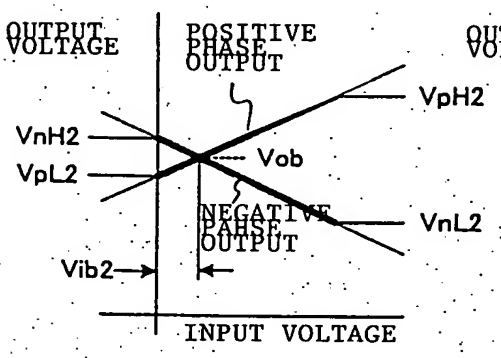
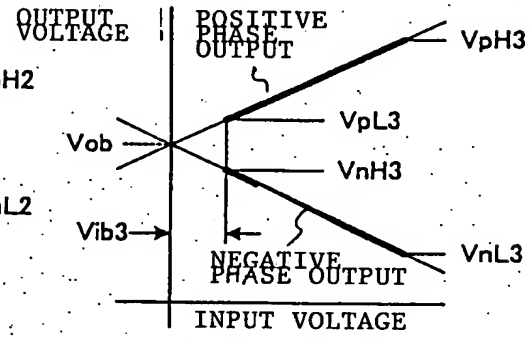


FIG. 5D



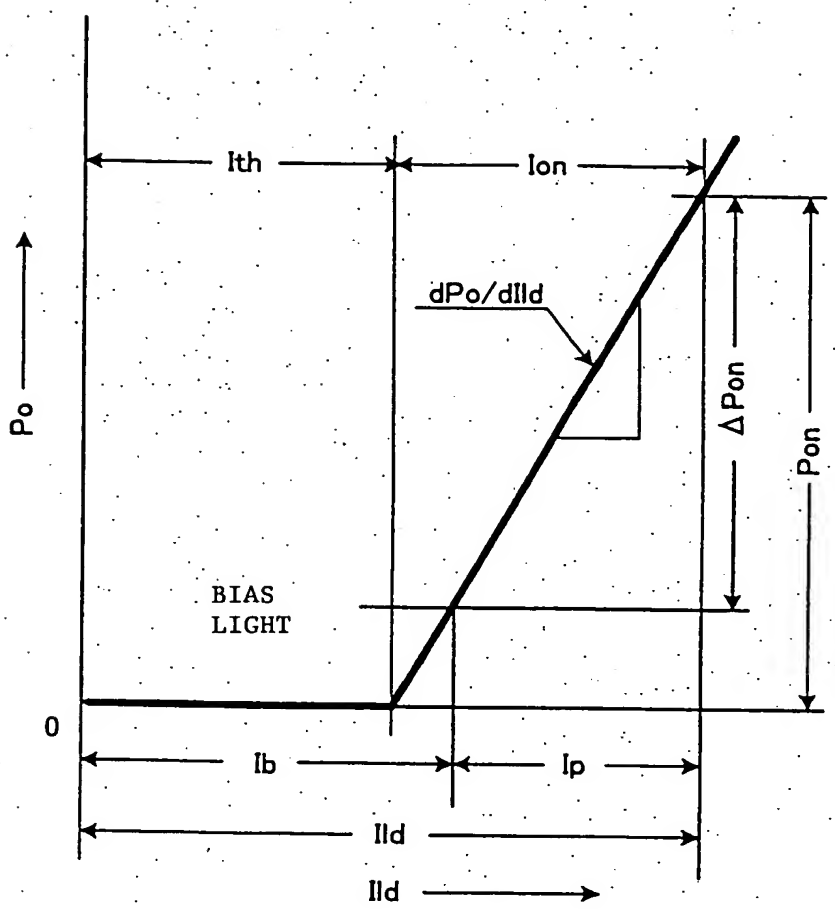


FIG. 6

FIG. 7A

ZERO OFFSET
SAME "1/0" RATIO
AC COUPLED INPUT

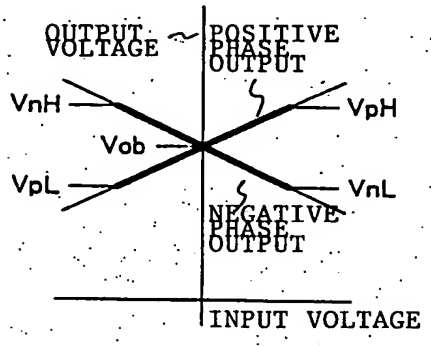


FIG. 7B

ZERO OFFSET
AC COUPLED INPUT

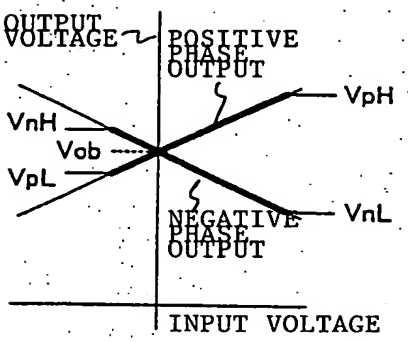
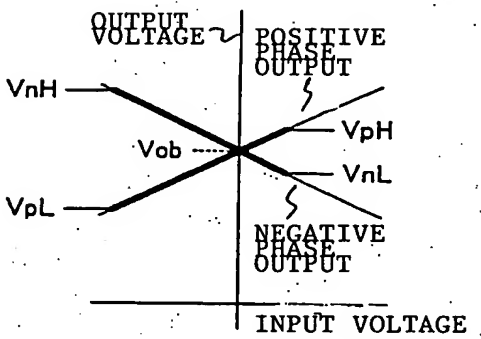


FIG. 7C

ZERO OFFSET
AC COUPLED INPUT



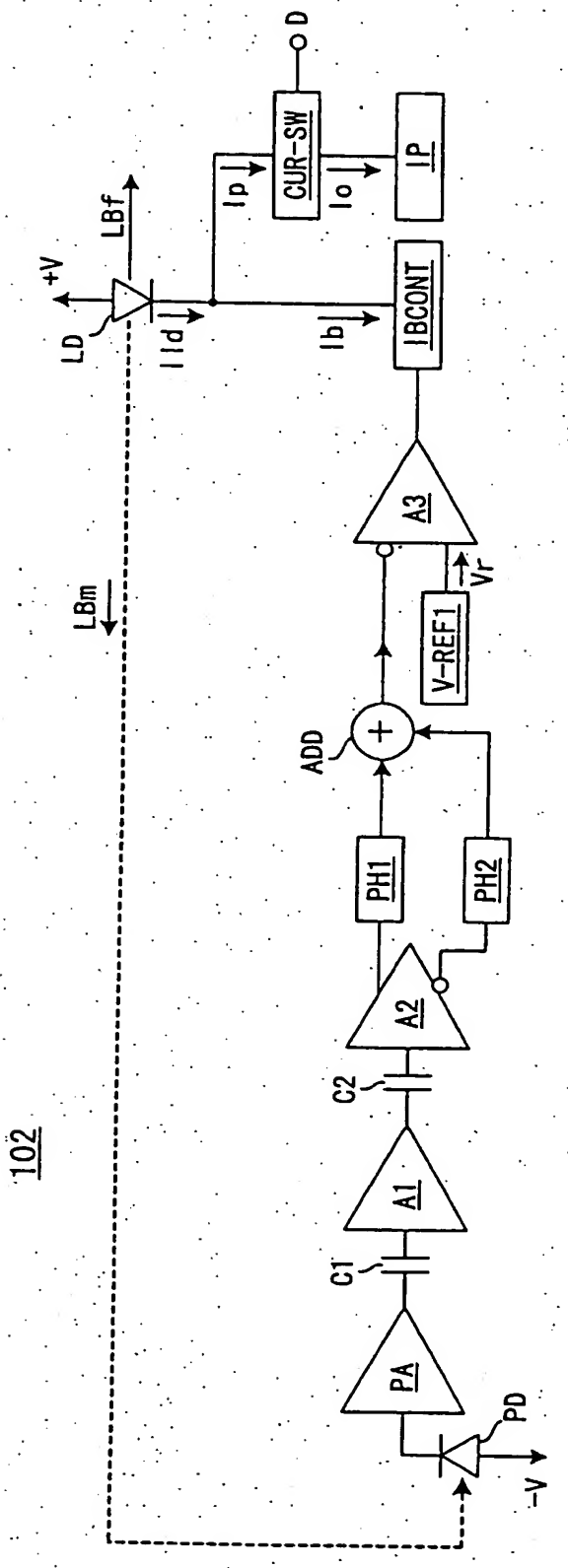

D
CUR-SW
IP
Ip
Io
LBf
+V
LD
Ild
Ib
IBCONT
A3
Vr
V-REF1
LBm
ADD
PH1
PH2
A2
C2
A1
C1
PA
PD
-V
102

FIG. 8

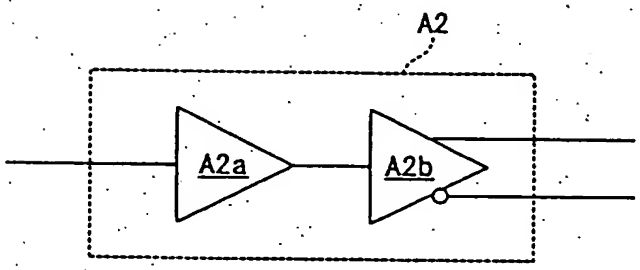


FIG. 9

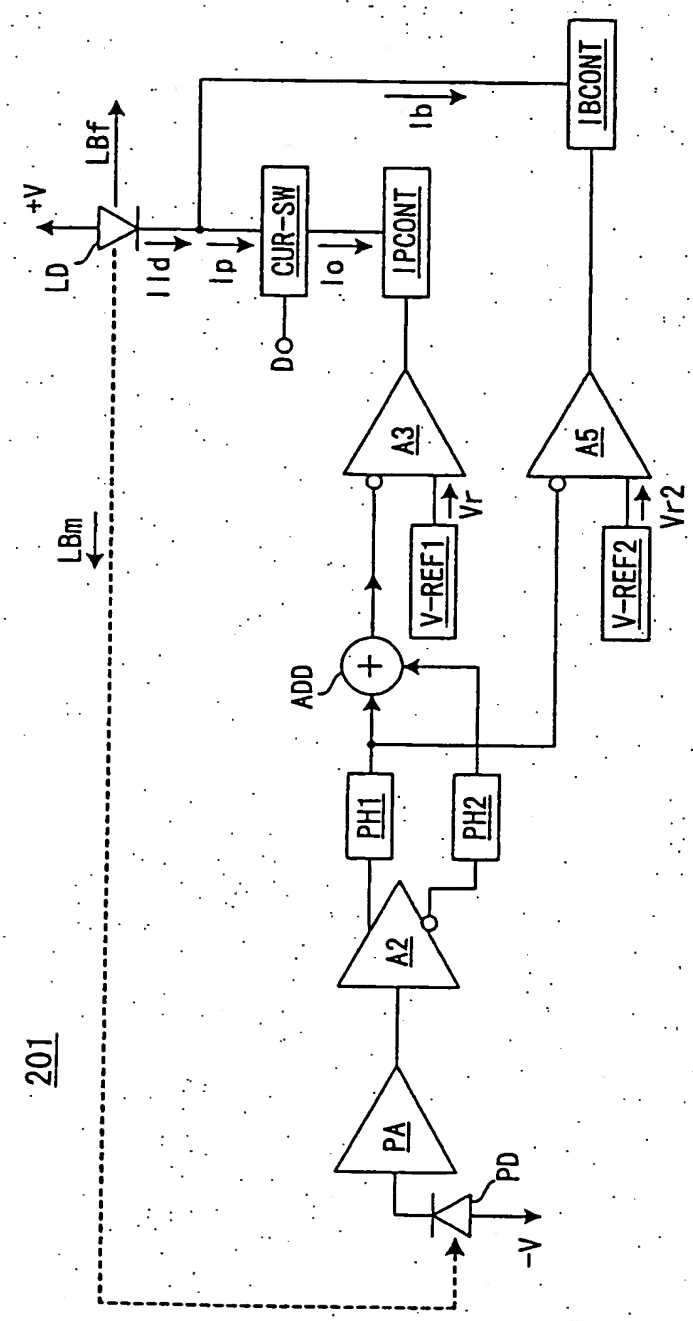

201
LD
+V
LBf
LBm
Ild
Ip
CUR-SW
Io
Do
IPCONT
Ib
IBCONT
A3
A5
Vr
Vr2
V-REF1
V-REF2
ADD
PH1
PH2
A2
PA
PD
-V

FIG. 10

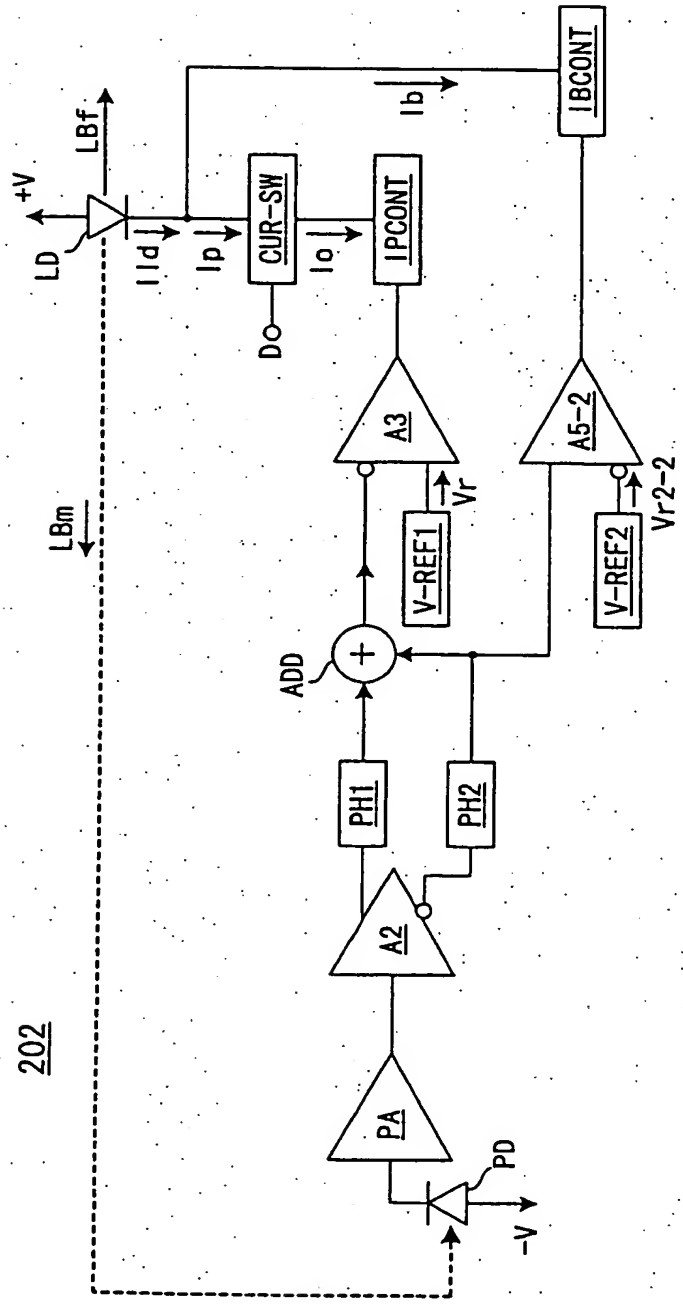

202
LD
+V
LBf
LBm
Ild
Ip
CUR-SW
Io
IPCONT
Ib
IBCONT
Do
A3
A5-2
Vr
Vr2-2
V-REF1
V-REF2
ADD
PH1
PH2
A2
PA
PD
-V

FIG. 11

FIG. 12A

ZERO OFFSET
Ib≒Ith (Ib>Ith)

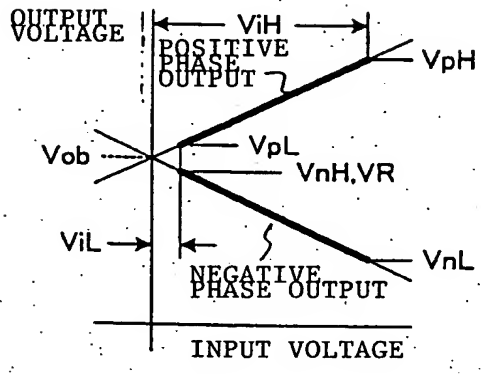


FIG. 12B

MINUS OFFSET
Ib>Ith

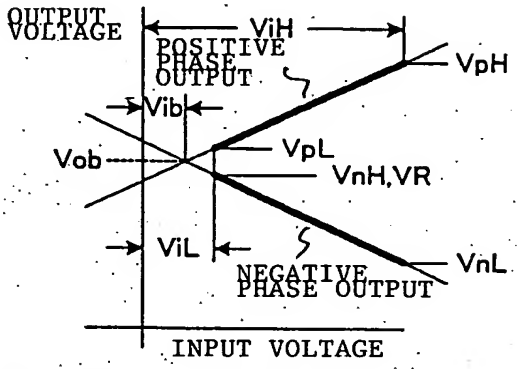


FIG. 12C

PLUS OFFSET
Ib>Ith ((LOW VR CASE)

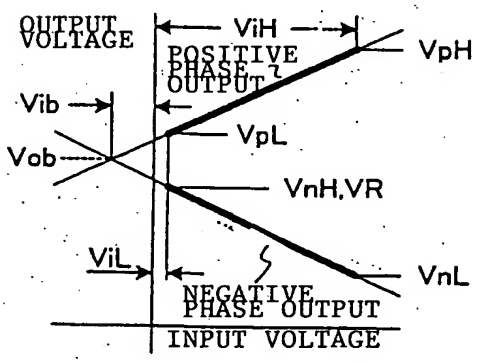
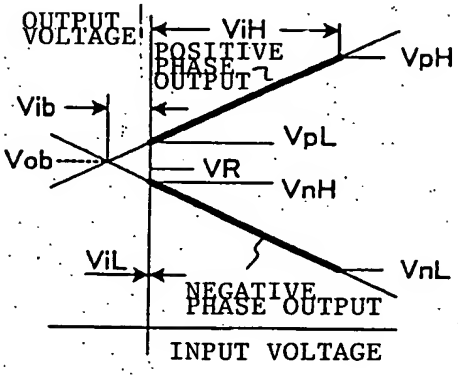


FIG. 12D

PLUS OFFSET
Ib=0 (HIGH VR CASE)



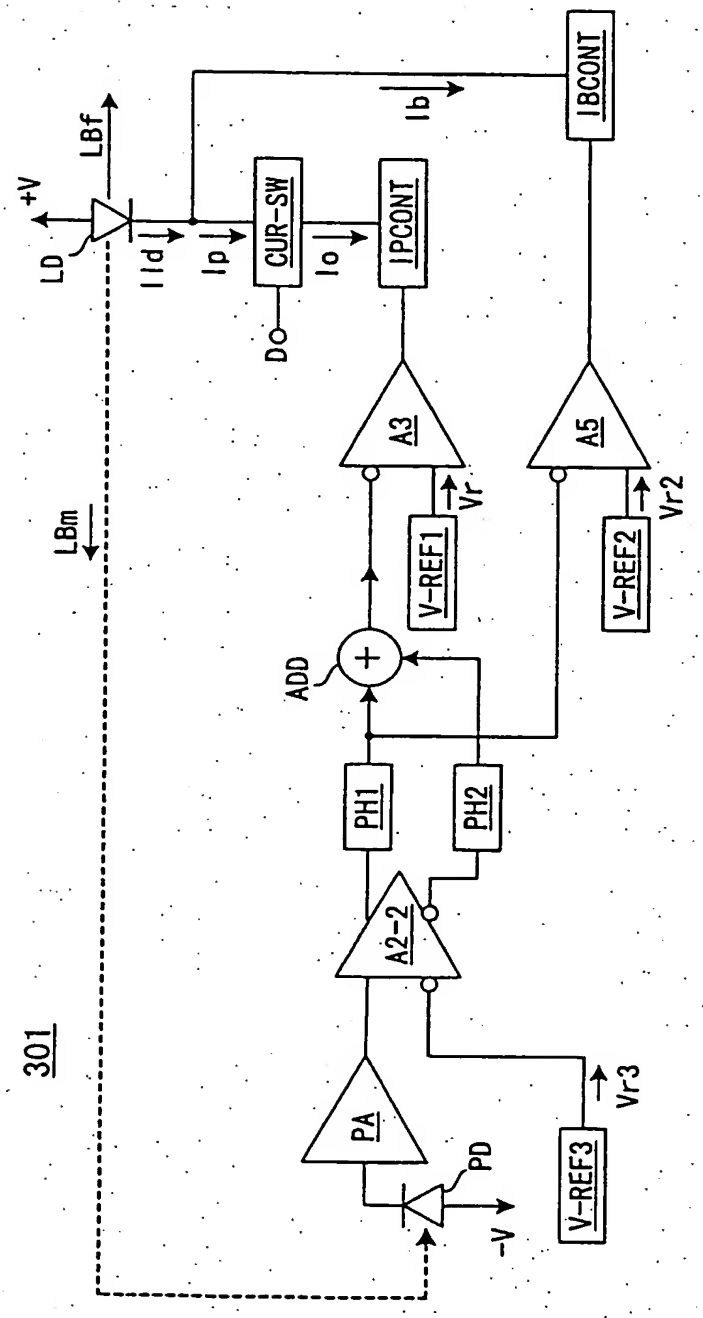

301
LD
+V
LBf
LBm
Ild
Ip
CUR-SW
Io
IPCONT
Ib
IBCONT
Do
A3
A5
Vr
Vr2
V-REF1
V-REF2
ADD
PH1
PH2
A2-2
PA
PD
-V
Vr3
V-REF3

FIG. 13

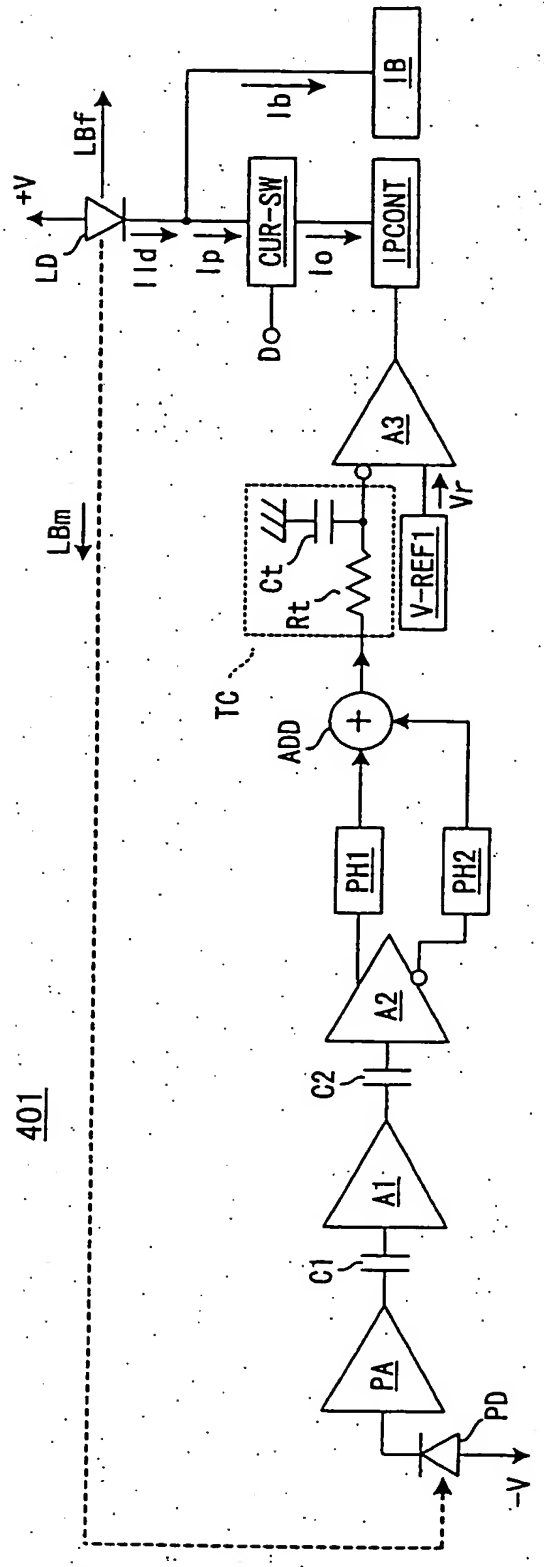

401
LBm
LBf
+V
LD
Ild
Ip
CUR-SW
Io
Ib
IB
IPCONT
Do
A3
Vr
V-REF1
Ct
Rt
TC
ADD
PH1
PH2
A2
C2
A1
C1
PA
PD
-V

FIG. 14

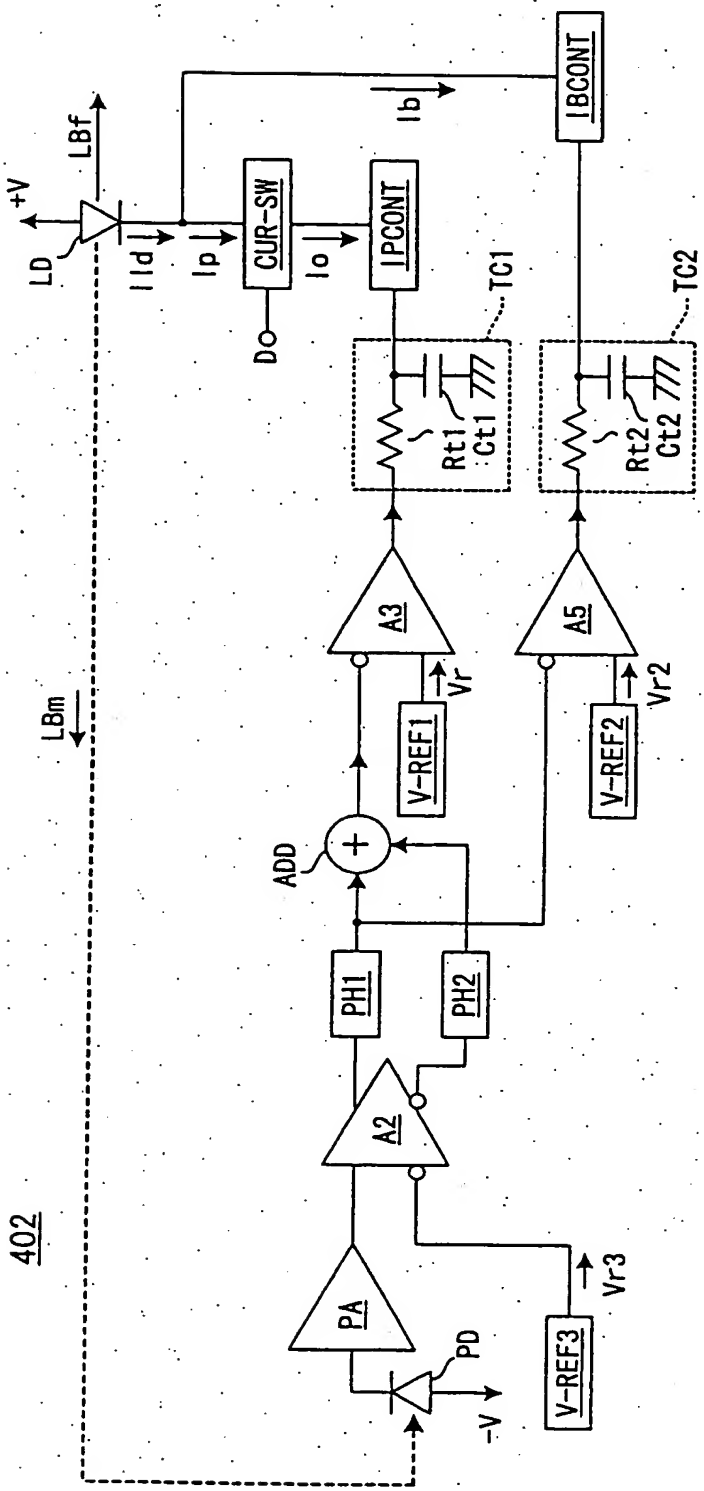

LBf
+V
LD
Ild
Ip
CUR-SW
Io
IPCONT
Ib
IBCONT
Do
TC1
TC2
Rt1
Ct1
Rt2
Ct2
A3
A5
Vr
Vr2
V-REF1
V-REF2
LBm
ADD
PH1
PH2
A2
PA
PD
-V
Vr3
V-REF3
402

FIG. 15

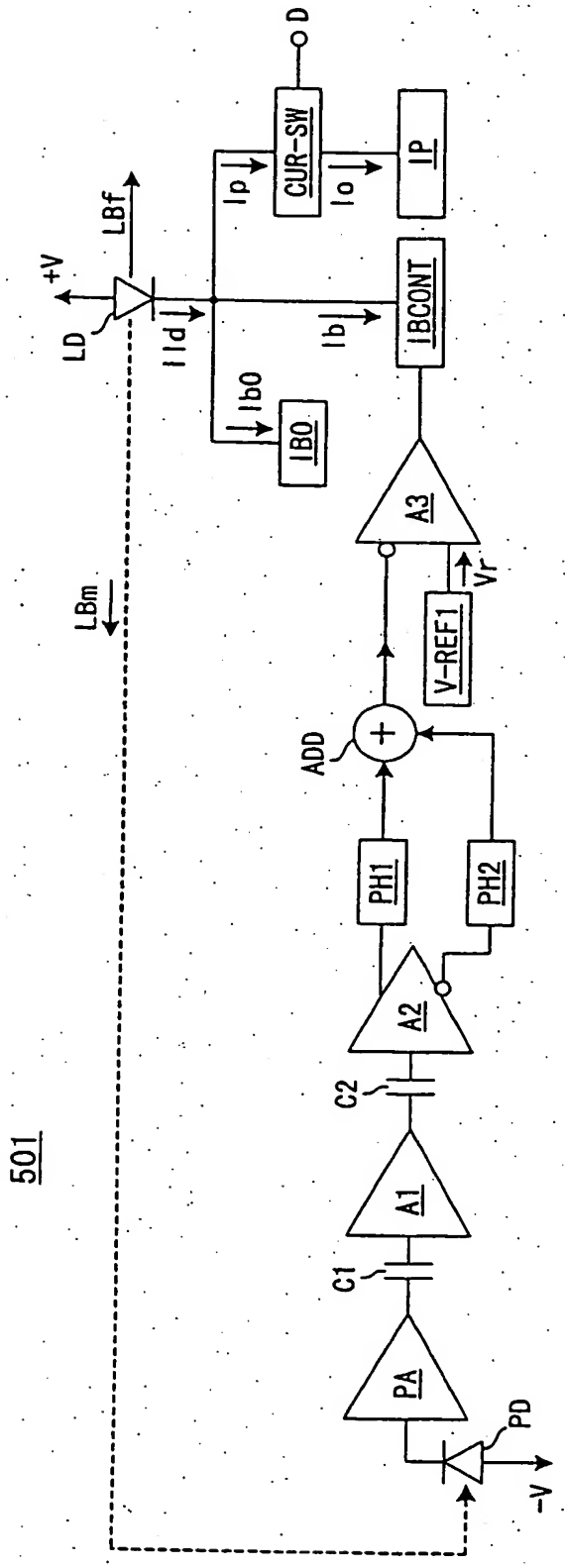

501
D
CUR-SW
IP
Ip
Io
LBf
+V
LD
Ild
Ib
IBCONT
Ibo
IBO
A3
Vr
V-REF1
LBm
ADD
PH1
PH2
A2
C2
A1
C1
PA
PD
-V

FIG. 16

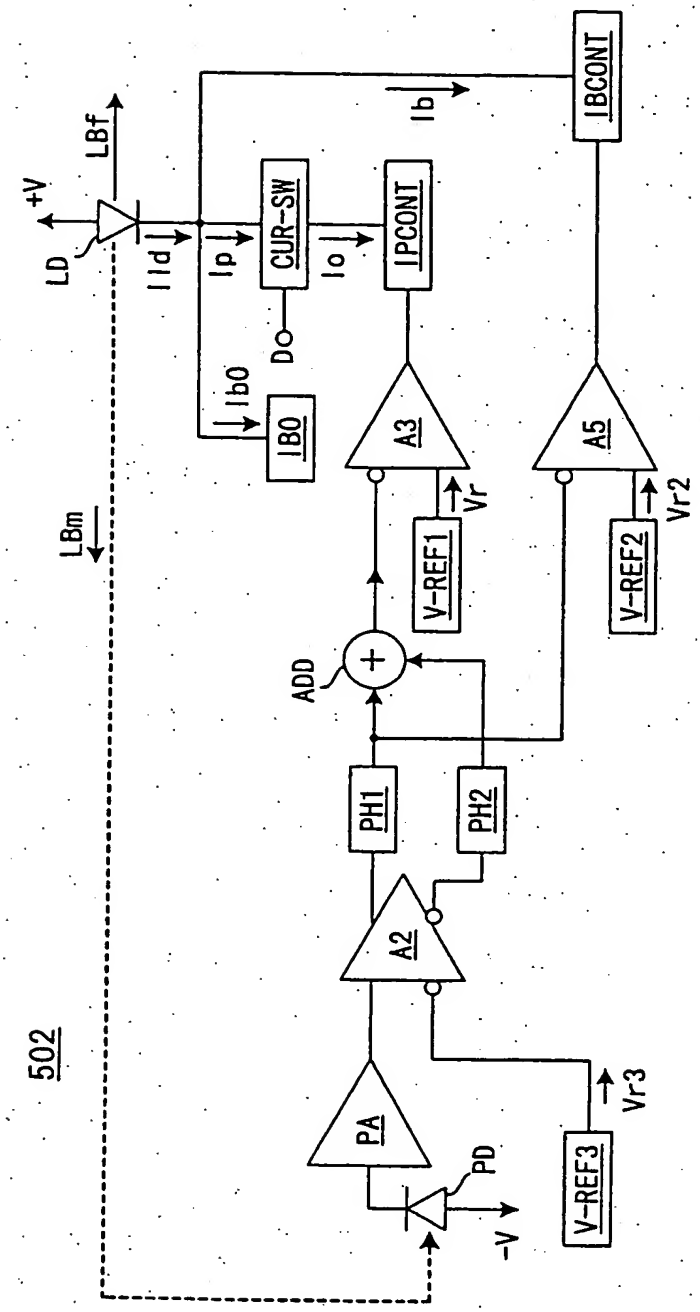

502
LD
+V
LBf
LBm
Ild
Ip
CUR-SW
Io
IPCONT
Ib
IBCONT
Do
IbO
IBO
A3
A5
Vr
Vr2
V-REF1
V-REF2
ADD
PH1
PH2
A2
PA
PD
-V
Vr3
V-REF3

FIG. 17

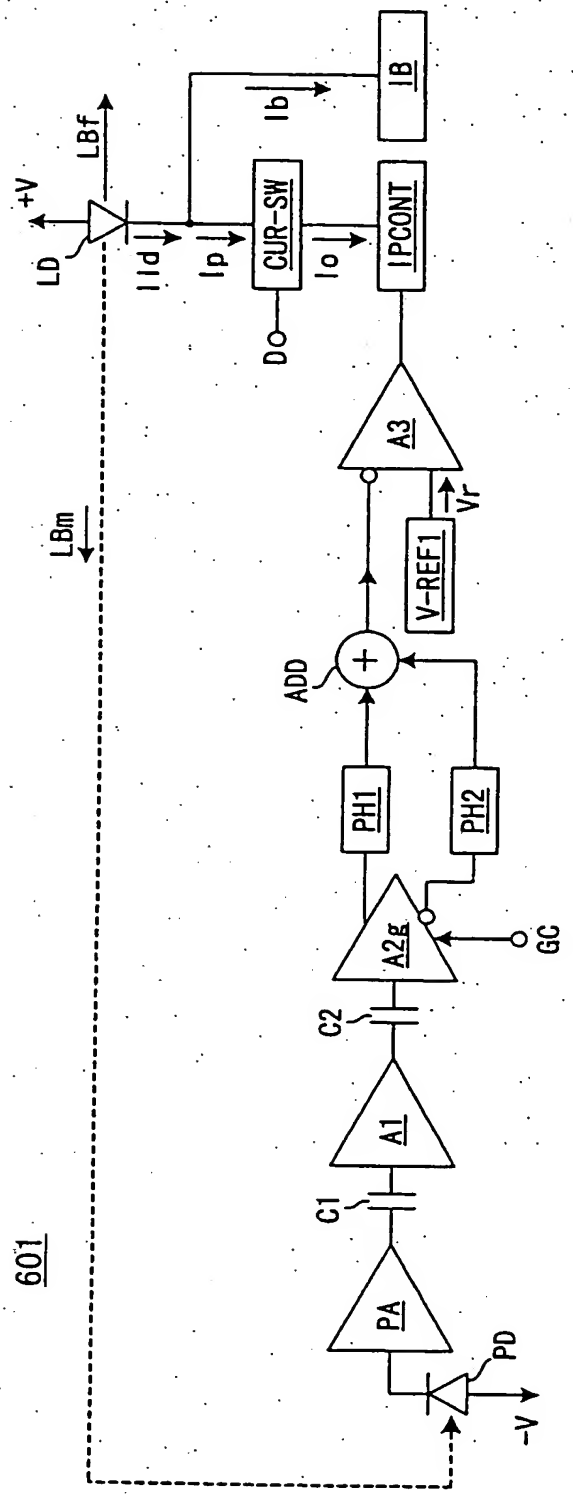

601
LD
+V
LBf
LBm
Ild
Ip
Io
Ib
IB
CUR-SW
IPCONT
DO
A3
Vr
V-REF1
ADD
PH1
PH2
A2g
GC
C2
A1
C1
PA
PD
-V

FIG. 18

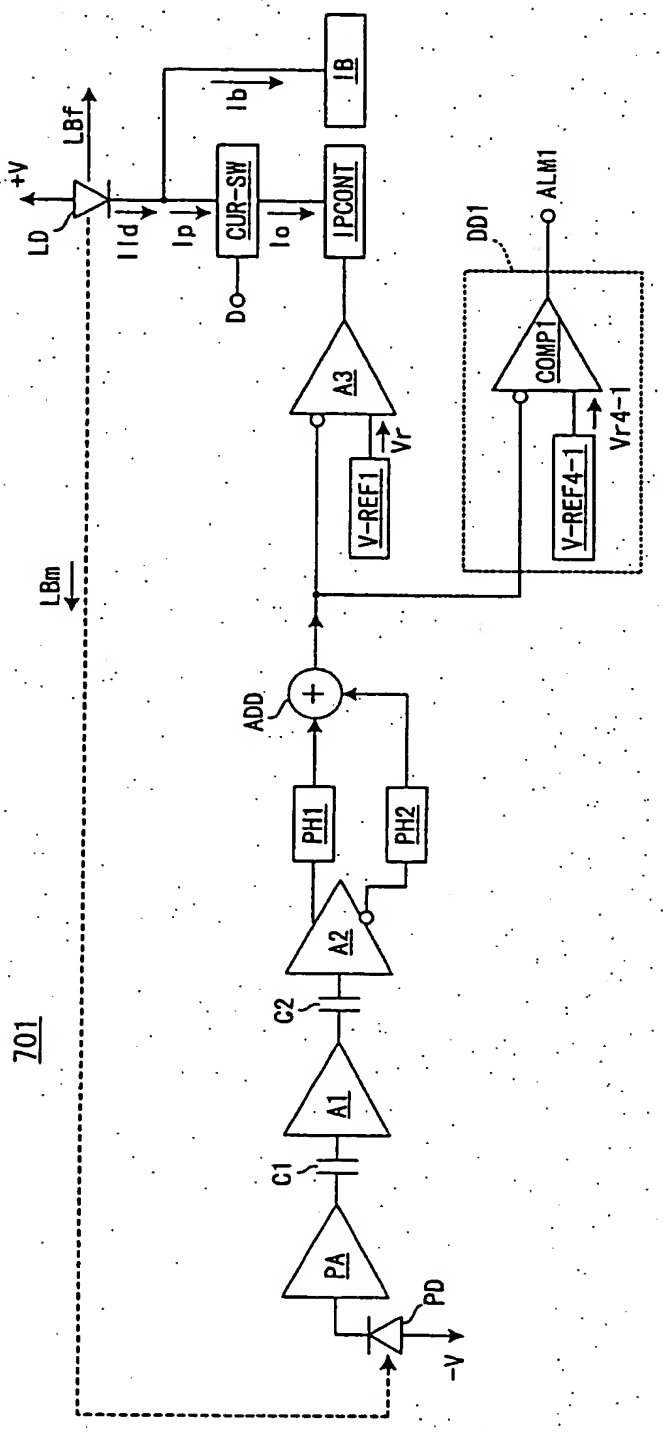

701
LD
+V
LBf
Ild
Ip
CUR-SW
Io
IPCONT
Ib
IB
Do
A3
Vr
V-REF1
DD1
ALM1
COMP1
Vr4-1
V-REF4-1
LBm
ADD
PH1
PH2
A2
C2
A1
C1
PA
PD
-V

FIG. 19

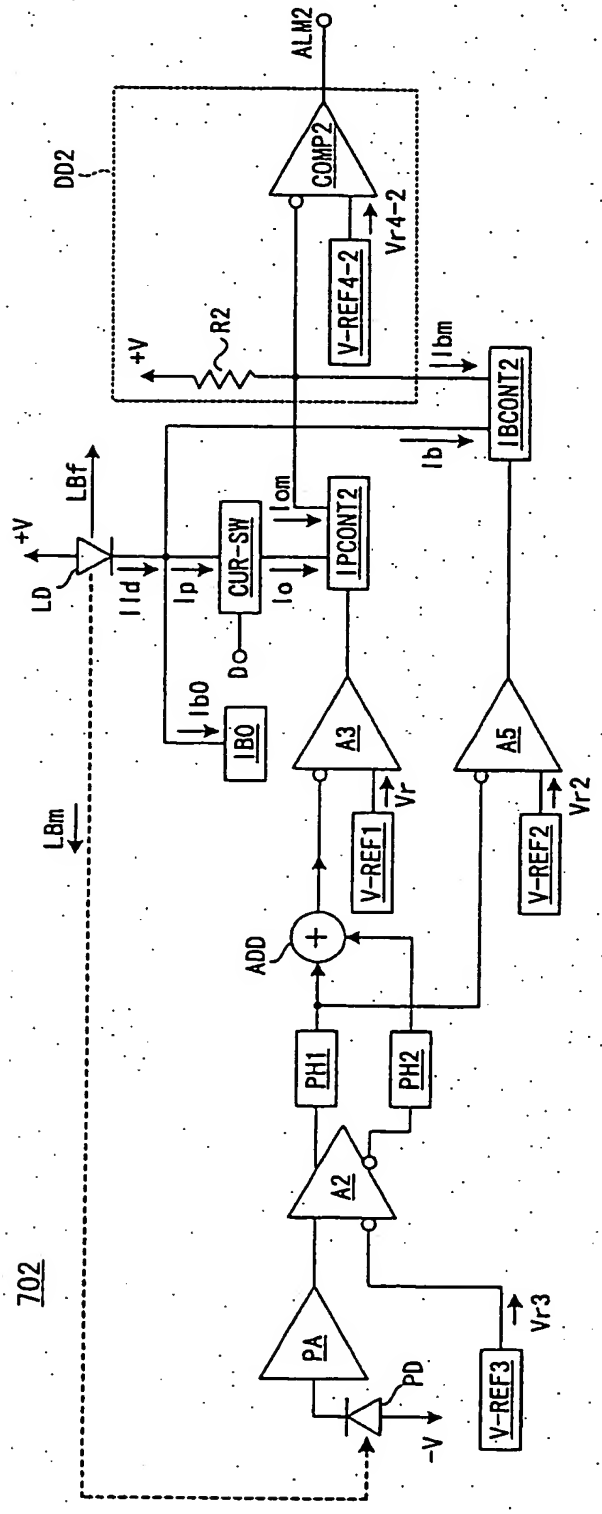

ALM2
COMP2
DD2
Vr4-2
V-REF4-2
R2
+V
Ibm
IBCONT2
Ib
LBf
+V
LD
Iid
Ip
CUR-SW
Iom
IPCONT2
Io
Do
Ibo
IBO
A3
A5
Vr
Vr2
V-REF1
V-REF2
LBm
ADD
PH1
PH2
A2
Vr3
PA
PD
-V
V-REF3
702

FIG. 20

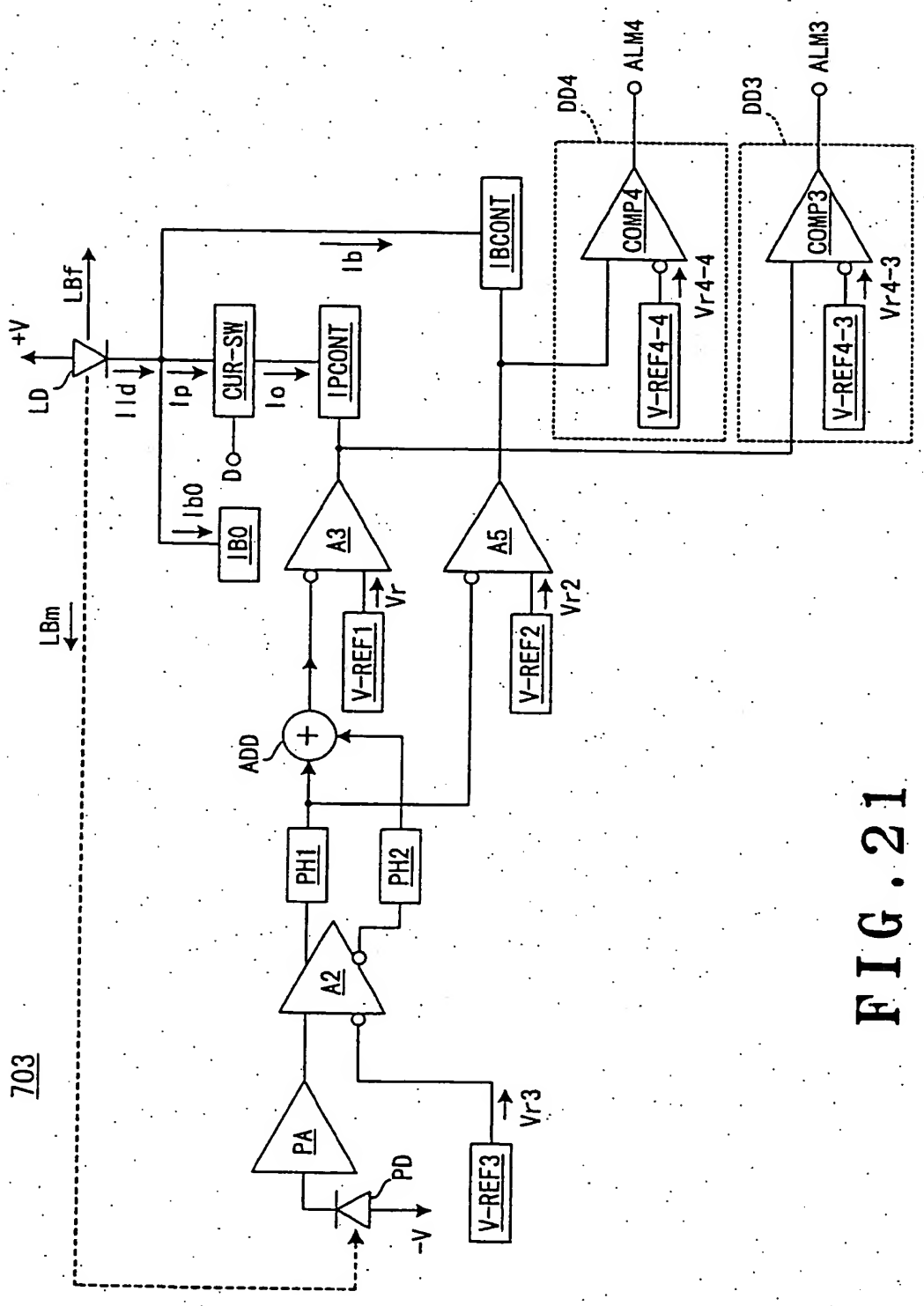

703
LD
+V
LBf
LBm
Ild
Ip
CUR-SW
Io
IPCONT
Ib
IBCONT
Do
IbO
IBO
A3
A5
Vr
V-REF1
Vr2
V-REF2
ADD
PH1
PH2
A2
PA
PD
-V
V-REF3
Vr3
DD4
ALM4
COMP4
V-REF4-4
Vr4-4
DD3
ALM3
COMP3
V-REF4-3
Vr4-3

FIG.21

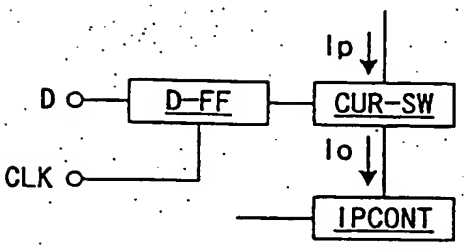


FIG. 22

FIG. 23A

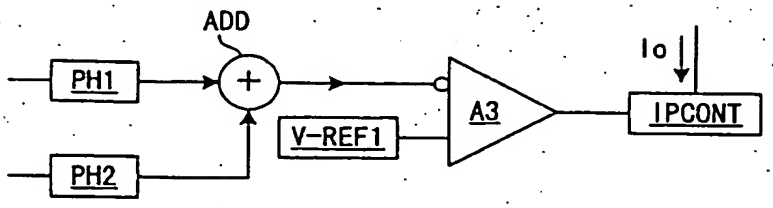


FIG. 23B

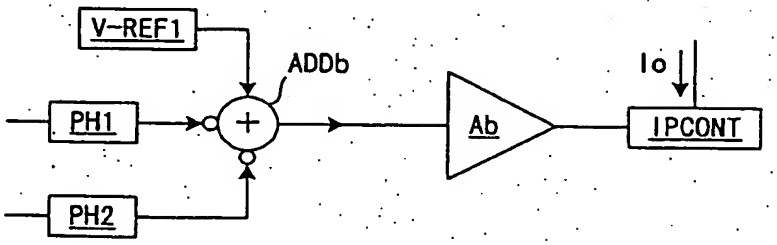


FIG. 23C

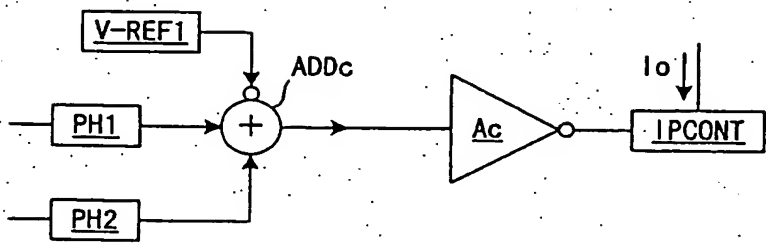


FIG. 23D

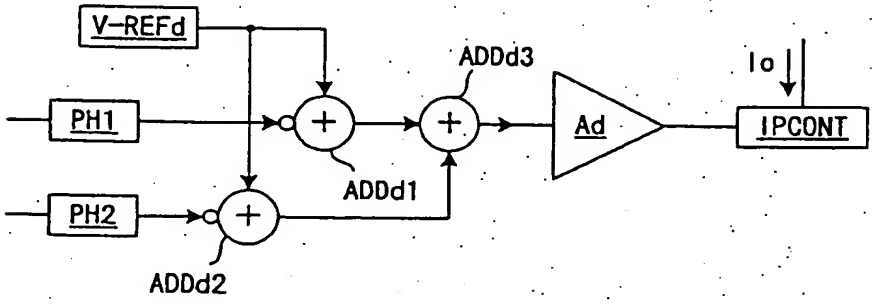


FIG. 24A

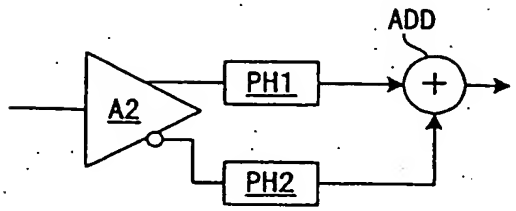


FIG. 24B

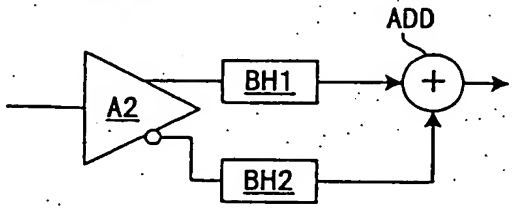


FIG. 24C

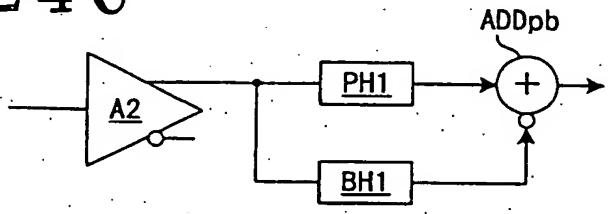


FIG. 25

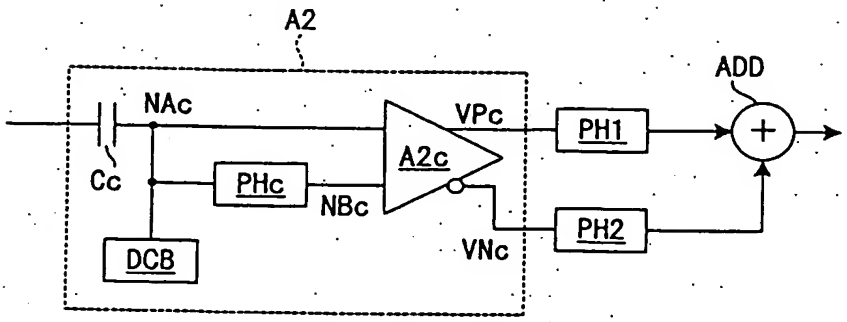


FIG. 26

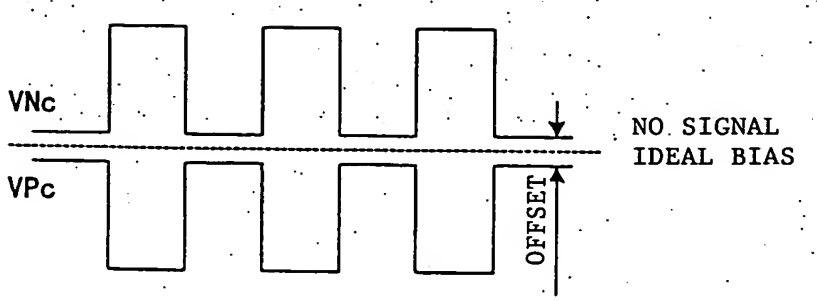
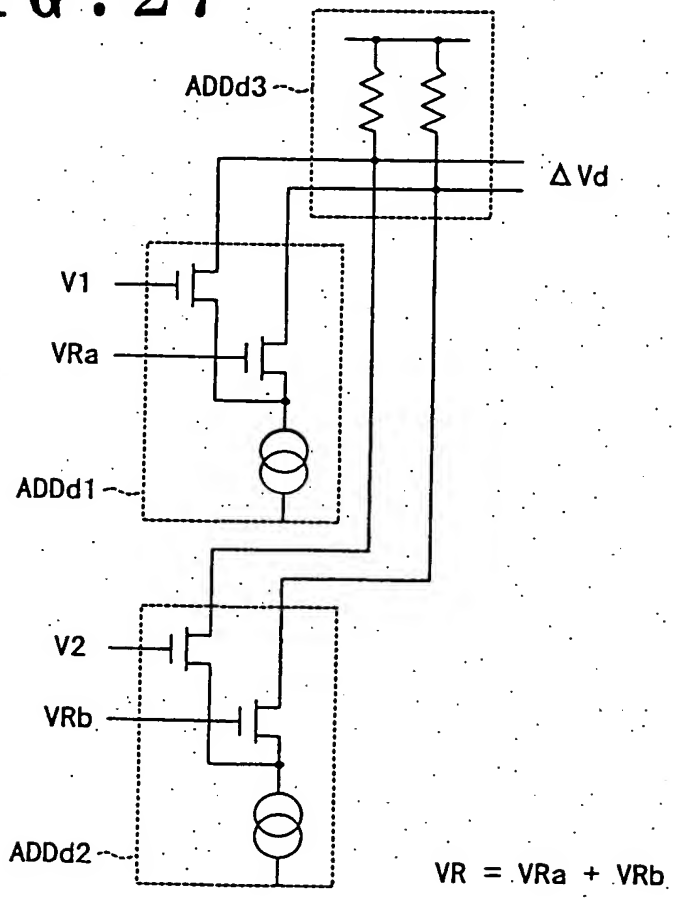

VNc
VPc
NO SIGNAL
IDEAL BIAS
OFFSET

FIG. 27


ADDd3
ΔVd
V1
VRa
ADDd1
V2
VRb
ADDd2
VR = VRa + VRb